CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the letters Patent is:

1. A method of improving the SiGe bipolar yield of a SiGe heterojunction bipolar transistor comprising the steps of:

(a) forming a passivation layer on at least exposed sidewalls of an emitter, said emitter is in contact with an underlying SiGe base region through an emitter opening formed in an insulator layer; and

(b) siliciding exposed silicon surfaces so as to form silicide regions therein.

2. The method of Claim 1 wherein said passivation layer is formed from a rapid thermal chemical vapor deposition process.

3. The method of Claim 1 wherein said passivation layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

4. The method of Claim 1 wherein said passivation layer is a nitride passivation layer.

5. The method of Claim 4 wherein said nitride passivation layer is formed from a rapid thermal chemical vapor deposition process which is carried out in a nitrogen-containing atmosphere.

6. The method of Claim 5 wherein said nitrogen-containing atmosphere is selected from the group consisting of NO, N_2O and N_2.

7. The method of Claim 4 wherein said rapid thermal chemical vapor deposition process is carried out at a temperature of about 700°C or greater.

8. The method of Claim 1 wherein said SiGe base region is formed by a deposition process selected from the group consisting of ultra-high vacuum chemical vapor

deposition (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition (RTCVD) and plasma-enhanced chemical vapor deposition.

9. A SiGe heterojunction bipolar transistor comprising:

a semiconductor substrate having a collector and subcollector region formed therein, wherein said collector is formed between isolation regions that are also present in the substrate;

a SiGe layer formed on said substrate, said SiGe layer including polycrystalline Si regions formed above said isolation regions and a SiGe base region formed above said collector and subcollector regions;

a patterned insulator layer formed on said SiGe base region, said patterned insulator layer having an opening therein;

an emitter formed on said patterned insulator layer and in contact with said SiGe base region through said opening, said emitter having exposed sidewalls;

a conformal passivation layer formed on at least said exposed sidewalls of said emitter; and

silicide regions formed on exposed portions of said SiGe layer and said emitter not covered by said conformal passivation layer.

10. The SiGe heterojunction bipolar transistor of Claim 9 wherein said semiconductor substrate is selected from the group consisting of Si, Ge, SiGe, GaAs, InAs, InP, other III/V compound semiconductors, Si/Si and Si/SiGe.

11. The SiGe heterojunction bipolar transistor of Claim 9 wherein said emitter is composed of intrinsic polysilicon.

12. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned insulator is composed of SiO_2 or Si oxynitride.

13. The SiGe heterojunction bipolar transistor of Claim 9 wherein said patterned insulator is composed of multi-insulator layers.

14. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is also formed on vertical sidewalls of said patterned insulator and portions of said SiGe base region.

15. The SiGe heterojunction bipolar transistor of Claim 9 wherein said silicide regions are formed in an exposed horizontal surface of said emitter, said polycrystalline Si region and a portion of said SiGe base region.

16. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is composed of a nitride, an oxide, an oxynitride or any combination thereof.

17. The SiGe heterojunction bipolar transistor of Claim 9 wherein said passivation layer is a nitride passivation layer.